CHIPS JOINT UNDERTAKING

Jari Kinaret

February 20, 2024

EUROPEAN PARTNERSHIP

WHAT IS CHIPS JOINT UNDERTAKING?

Public-private partnership (PPP)

Partnerships between public authorities and industry intend to bring project results closer to the market and improve the link between research and societal growth. The PPPs are based on long term contracts that can take many different legal forms, from contractual partnerships to specific legal entities.

Joint undertaking (JU)

A Joint Undertaking is an institutionalized PPP with its own legal identity, with its own governance, budget etc.. The JUs are established by an EU regulation.

Chips JU

Chips JU was established in September, 2023, in an amendment to the Single Basic Act to implement the first pillar of the Chips Act and to continue the activities of its predecessors in the field of electronic components and systems (ECS). The Chips JU is a tri-partite partnership between the EC, the participating states and European industries; most of our actions are funded jointly and equally by these actors.

Chips Act: Entry into force, 21 September 2023
Signatures 13 September, Publication 18 September 2023

Roberta Metsola (European Parliament President)
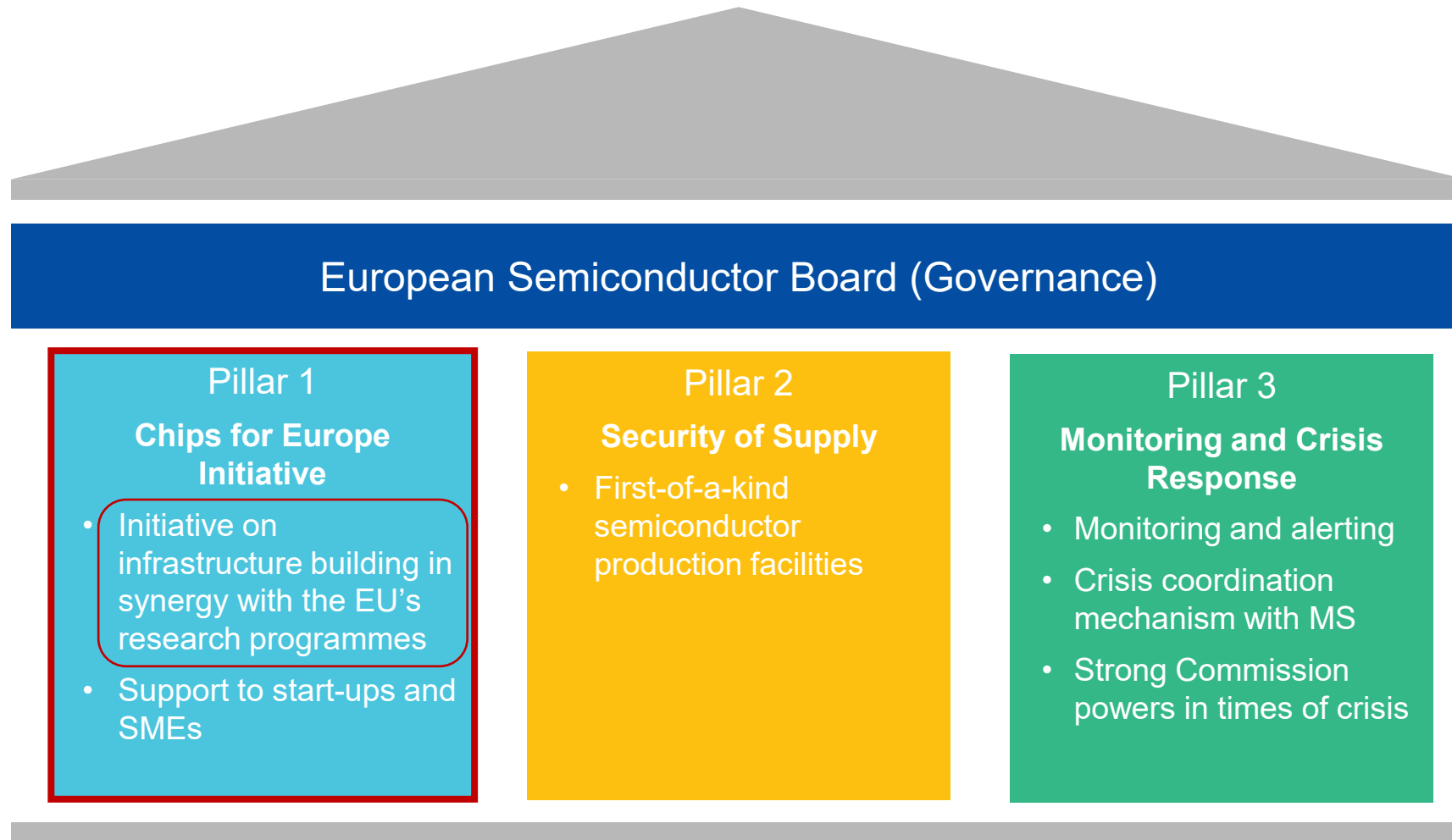José Manuel Albares Bueno (Council Presidency)

Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

EUROPEAN PARTNERSHIP

THE 3 PILLARS OF THE CHIPS ACT

European Semiconductor Board (Governance)

Pillar 1
Chips for Europe Initiative

- Initiative on infrastructure building in synergy with the EU's research programmes
- Support to start-ups and SMEs

Pillar 2
Security of Supply

- First-of-a-kind semiconductor production facilities

Pillar 3
Monitoring and Crisis Response

- Monitoring and alerting
- Crisis coordination mechanism with MS
- Strong Commission powers in times of crisis

Chips JU and its predecessor Key Digital Technologies JU (KDT JU)

Non-initiative

- **KDT General Objectives**
  a) Reinforce EU strategic autonomy in electronic components and systems
  b) Establish EU scientific excellence and innovation leadership
  c) Ensure that components and systems technologies address Europe's societal and environmental challenges

Initiative

- **From KDT to Chips JU**
  d) Pilot lines
  e) Design platform
  f) Competence centers
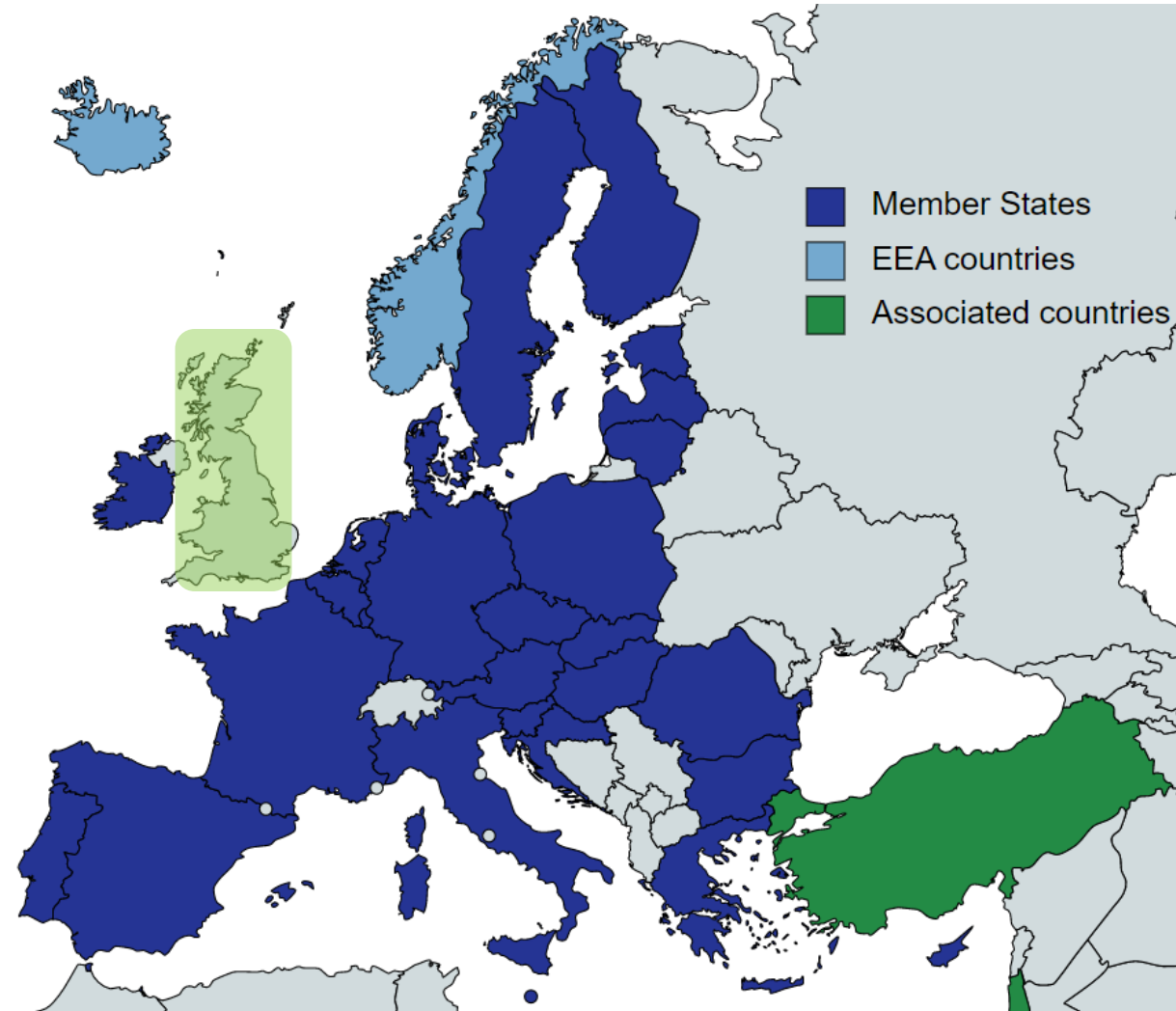 g) Quantum chips technology
  Digital Europe Programme in addition to Horizon Europe

- **Disclaimed:** *we know that the WP2023-2027 will need to be updated/amended in the spring and some details on the following pages may change:*
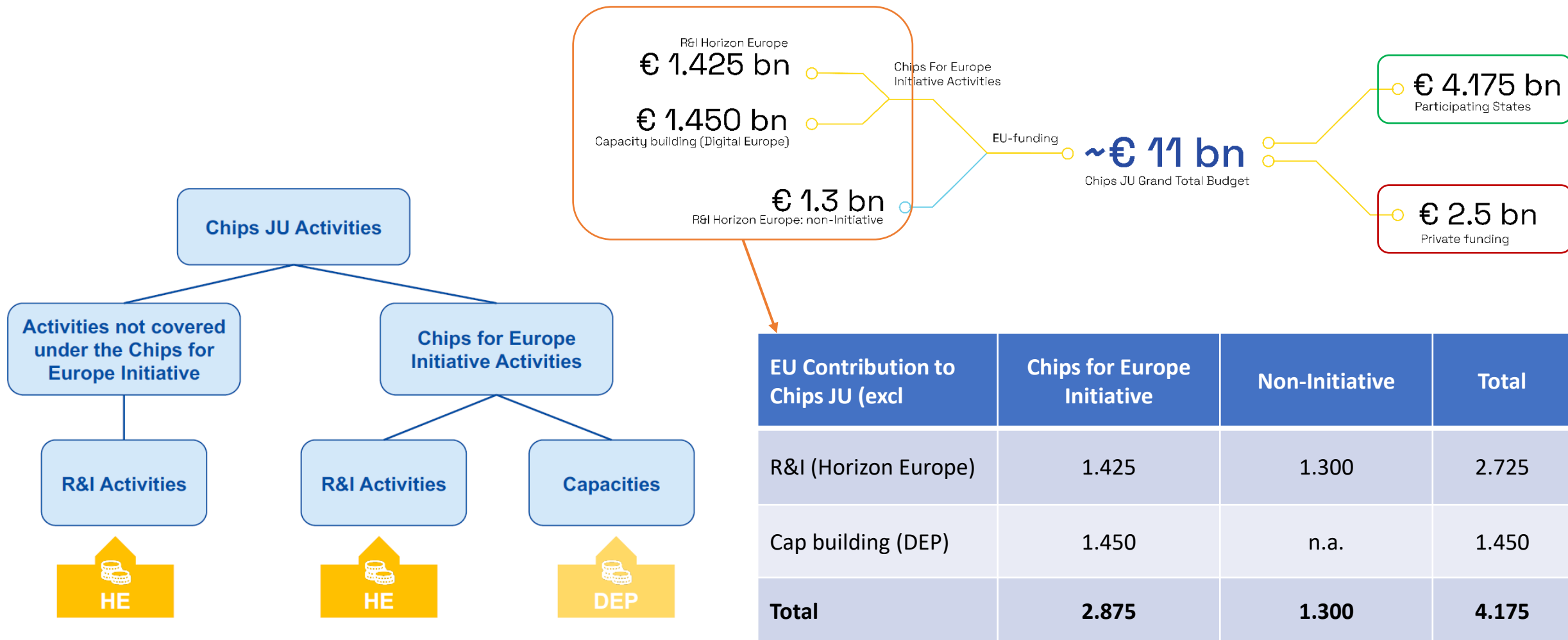 https://www.chips-ju.europa.eu/Library/

- How to participate:
  https://www.chips-ju.europa.eu/Participate/

Legend:
- Member States (dark blue)
- EEA countries (light blue)
- Associated countries (green)

Chips JU

Chips JU Activities
- **Activities not covered under the Chips for Europe Initiative**
  - **R&I Activities** — HE
- **Chips for Europe Initiative Activities**
  - **R&I Activities** — HE
  - **Capacities** — DEP

R&I Horizon Europe
€ 1.425 bn

€ 1.450 bn
Capacity building (Digital Europe)

€ 1.3 bn
R&I Horizon Europe: non-Initiative

Chips For Europe Initiative Activities

EU-funding

~€ 11 bn
Chips JU Grand Total Budget

€ 4.175 bn
Participating States

€ 2.5 bn
Private funding

EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

Jari Kinaret – 20 February 2024

Chips JU None Initiative Calls

Anton Chichkov

March 04, 2024

CHIPS JU NONE INITIATIVE CALLS 2024

Action	Title	Maximum JU Funding (M€)
HORIZON-Chips 2024-1-IA-T1	Global IA call according to SRIA 2024	103.00
HORIZON-Chips 2024-1-IA-T2	Focus topic on "High Performance RISC-V Automotive Processors supporting SDV"	20.00
HORIZON-Chips 2024-1-IA-T3	Focus topic on "Service Oriented Framework for the Software Defined Vehicle of the future"	20.00
HORIZON- Chips 2024-2-RIA-T1	Global RIA call according to SRIA 2023	52.00
HORIZON- Chips 2024-2-RIA-T2	Focus topic on "Sustainable and greener manufacturing"	15.00
HORIZON- Chips 2024-3-RIA	Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems	6.00
		216.00

Chips JU IA proposals

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industry led consortium**
- Developing **innovative technologies and/or using them in innovative ways**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- IA Prjects should contribute to, short to midterm **economic value creation** in Europe

Focus topic on High Performance RISC-V Automotive Processors Supporting SDV

- RISC-V still requires important extensions and add-ons in order to support *high-performance automotive quality processing* needs.

  - Efforts should be focussed on the development of an **automotive RISC-V reference hardware platform**.

  - **Open-source RISC-V based hardware** system implementation of the **SDV Hardware Layer** compatible with one or multiple widely-agreed-upon **Hardware Abstraction Layers** of the vehicle of the future is targeted.

  - The expected RISC-V reference platform shall be targeted for **commercial use** and should comply with **industry standards** especially with respect to quality and safety.

  - It should contain all assets needed to enable the adoption of RISC-V cores throughout the European automotive ecosystem.

Focus topic on Software-define vehicle middleware and API framework for the vehicle of the future

- Europe needs to join forces in order to lead on the Software Defined Vehicle (SDV) technology

- The SDV software stack should be extended by a **Middleware and Application Programming Interface (API) Framework**

  - **To** supports different technologies.

  - This framework should expose the hardware functionalities directly as APIs or services

  - This car OS should be independent, standardized & interoperable, as well as safe, secure, efficient and easily accessible

- This call has a focus on

  - *Modular (open-source) building blocks*

  - *Open architectures* of the *SDV middleware and API framework* for the *vehicle of the future*.

  - *Holistic engineering framework*

Chips JU RIA proposals

- RIA proposal is characterized by

  - The activities have their centre of gravity at **TRL 3-4**

  - Execution normally by an **academy led consortium**

  - Developing **innovative disruptive technologies**

  - Targeting **demonstration of the innovative approach**, clearly addressing relevant societal challenges

  - Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application

  - Having a **deployment plan showing the valorisation for the ECS ecosystem** and the contribution to the Chips JU goals and objectives

Focus Topic Sustainable and Greener Manufacturing

- This focus topic concerns the development of a **sustainable and greener semiconductor manufacturing** through the reduction of its environmental footprint with a **focus on materials**. The results of the project are expected to contribute to the following outcomes:

  - Increase the use of **environmentally friendly materials**, chemicals and solvents.

  - **Minimization of waste** and emissions during production and processing

  - Prevention of a future scarcity of some critical materials for SC processing through a **more efficient and cost-effective products** and **electronic waste recycling** in process., including chips and PCBs.

Joint call with Korea

- This joint call for proposals between the Republic of Korea and the EU addresses the topics related to **Heterogeneous integration and neuromorphic computing technologies** for future semiconductor components and systems and intends to set a framework

  - To strengthen the relation between R&I players in both jurisdictions

  - To undertake joint R&I for EU and Korean R&I teams by cooperating in pre-competitive projects on areas which are in the interest of both jurisdictions.

  - To build trust for further cooperation.

- This joint call topic will be co-funded by South Korea (KR) and the European Union (EU)

- This call has very specific conditions. Please conslut the call text in the work programme

Chips JU

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EU Funding Rates

Type of beneficiary	2024-1-IA	2024-1-IA Focus Topics	2024-2-RIA	2024-2-RIA Focus Topic	2024-3-IA
Large Enterprise	20 %	25 %	25 %	25 %	100%
SME	30 %	30 %	35 %	35 %	100%
University/Other (not for profit)	35 %	35 %	35 %	35 %	100%
National Funding	YES	YES	YES	YES	NO

Schedule

Calls 2024-1 and 2024-2	Two stage Call with submission of Project Outline (PO) and Full Proposal (FPP)
Publication date	06 February 2024
Deadline PO Phase	14 May 2024 at 17:00 Brussels Time
Deadline FPP Phase	17 September 2024 at 17:00 Brussels Time
PAB selection	November 2024
Grant preparation	December 2024 to April 2025
Start of the projects	around May 2025

For the Call2024-3, there is no PO phase only an FPP phase with e deadline on 14 May 2024

Proposal Evaluation, Selection, and Grant Agreement Preparation

Column 1:

Submission of Project Outline Proposal
↓
Admissibility and eligibility check
↓
Evaluation by experts
↓
Feedback to coordinator

Column 2:

Submission of Full Project Proposal
↓
Admissibility and eligibility check
↓
Evaluation by experts
↓
Assessment by the PAB in relation with national priority
↓
Final proposal ranking (PAB)
↓
PAB Funding Decision
↓
Communication to coordinator

Column 3:

Start of JU GA preparation
↓
Start of national GA preparation
↓
Final funding figures
↓
Final DoA
↓
PAB final funding decision
↓
JU GA signature

Useful links

Check regularly the call information under the CHIPS website:

https://www.chips-ju.europa.eu/

Address eventual questions related to the calls to:

calls@chips-ju.europa.eu

Consult the sections on the 2024 calls in the:

Chips JU Work Programme

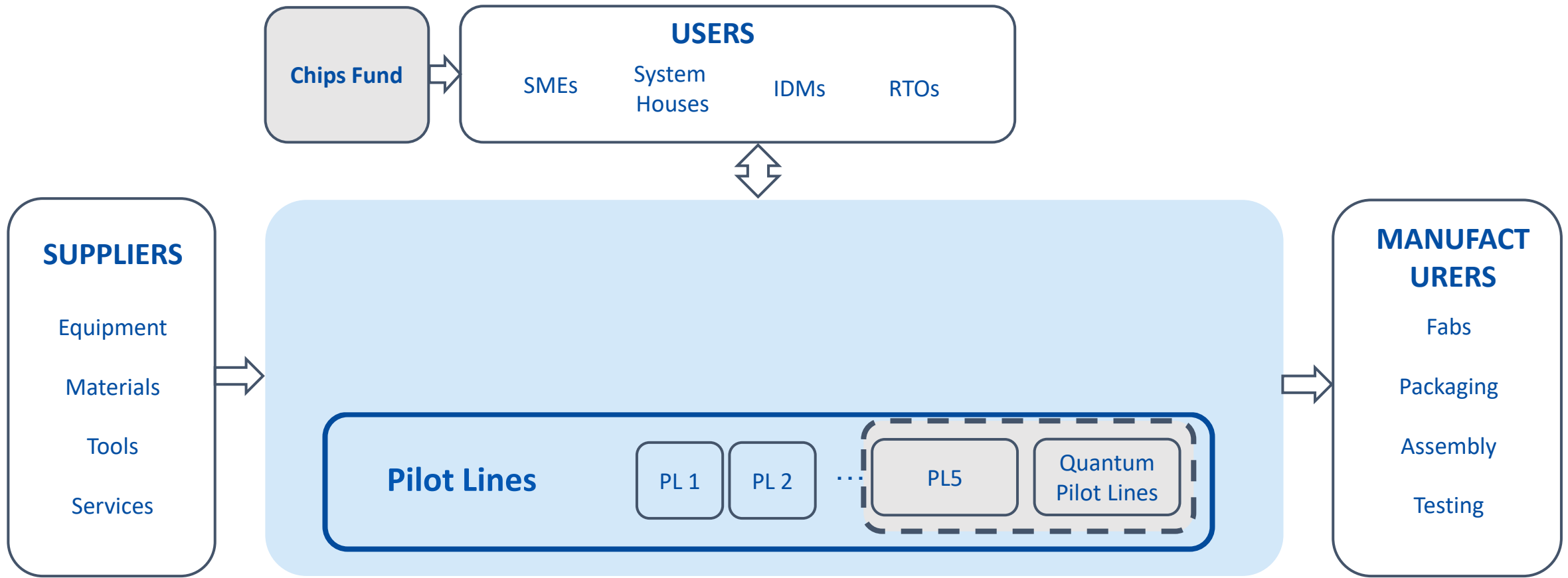# CHIPS JU INITIATIVE CALLS

Anton Chichkov

March 04, 2024

2. Chips JU Calls 2023- Initiative

Four Calls for Pilot Lines (CPL)

Pilot line	EU Budget
Pilot line on advanced sub 2nm leading-edge system on chip technology	700 million Euro
Pilot line on advanced Fully Depleted Silicon On Insulator technologies targeting 7nm	420 million Euro
Pilot line on advanced Packaging and Heterogenous Integration	370 million Euro
Pilot line on advanced semiconductor devices based on Wide Bandgap materials	180 million Euro

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Chips for Europe Initiative
From lab to fab

Chips for Europe Initiative
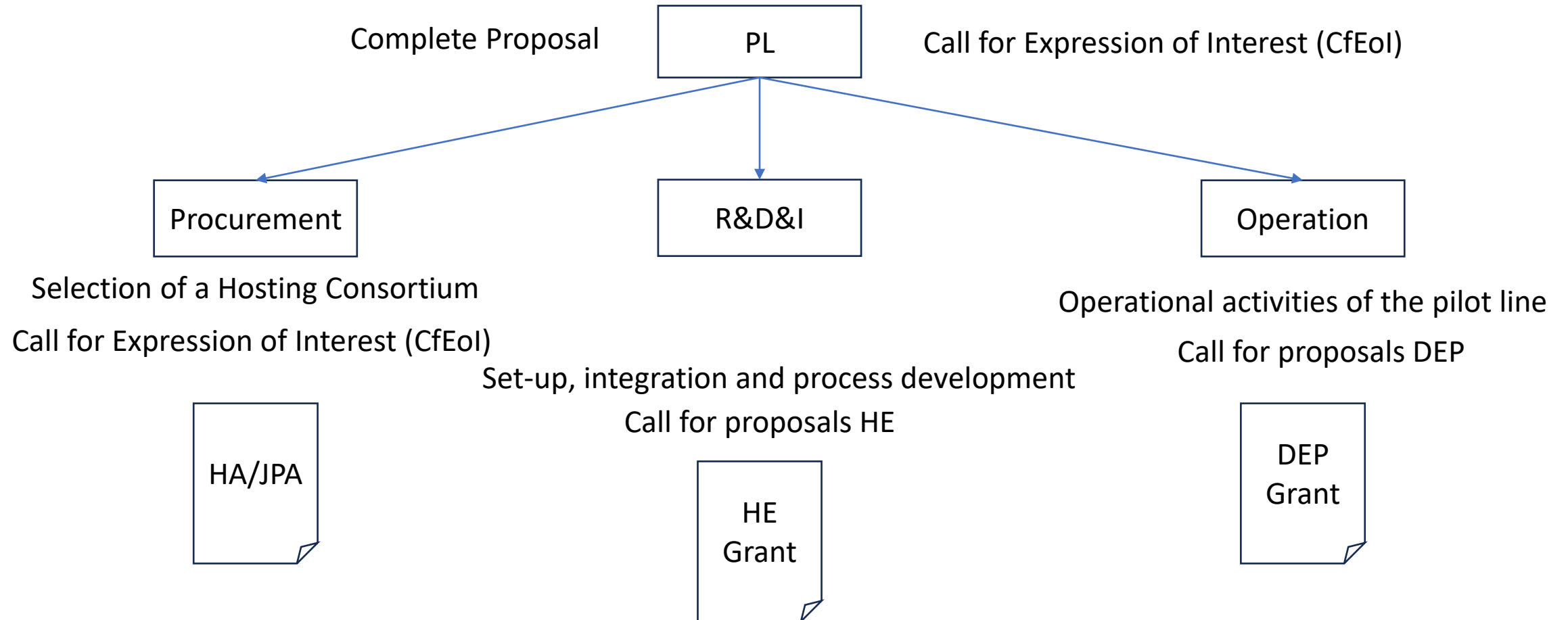From lab to fab
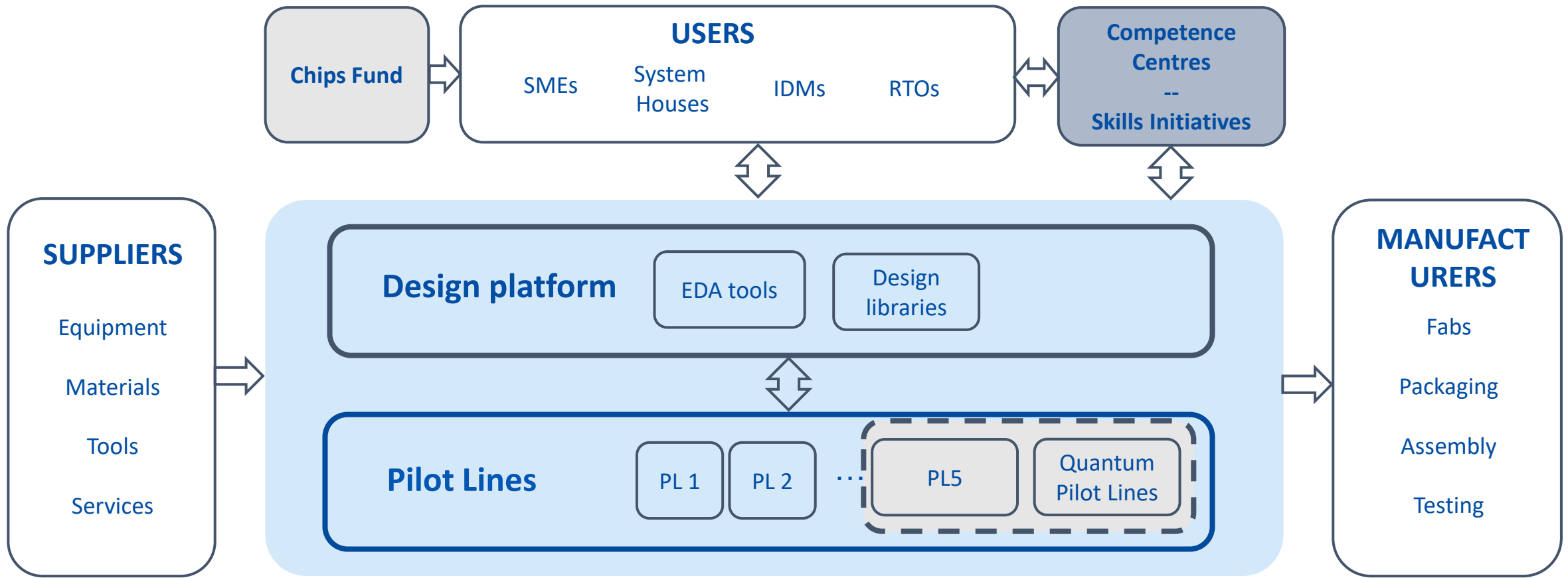
Chips for Europe Initiative
From lab to fab

Chips JU Pilot lines

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                              │    PL    │
                              └────┬─────┘
              ┌────────────────────┼────────────────────┐
              ▼                    ▼                     ▼
     ┌──────────────┐      ┌──────────────┐      ┌──────────────┐
     │ Procurement  │      │    R&D&I     │      │  Operation   │
     └──────────────┘      └──────────────┘      └──────────────┘
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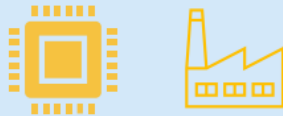
Procurement

Facilities
(existing and to be build)
Equipment
(existing and to be purchased)

… … …

R&D&I

Materials
Recipes
Methods
Technology modules,
Metrology,
Control systems

… … …

Operation
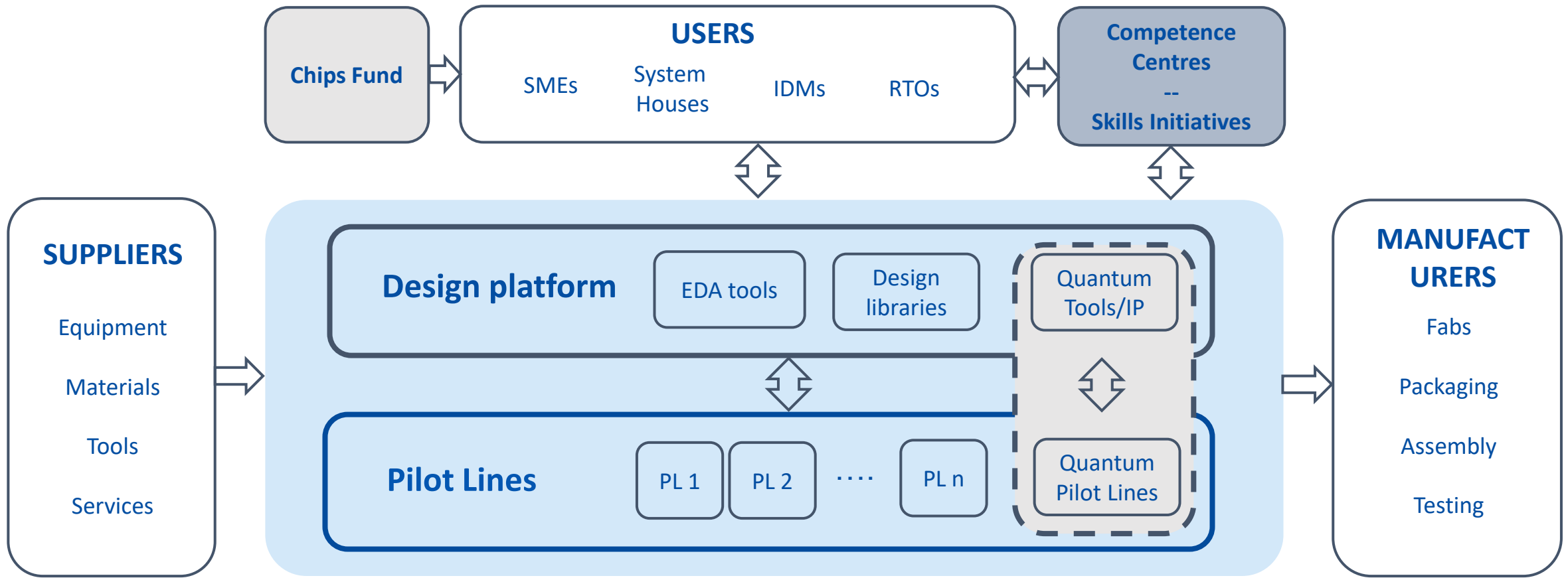
Offered technologies
Services
Capacity
Access

… … …
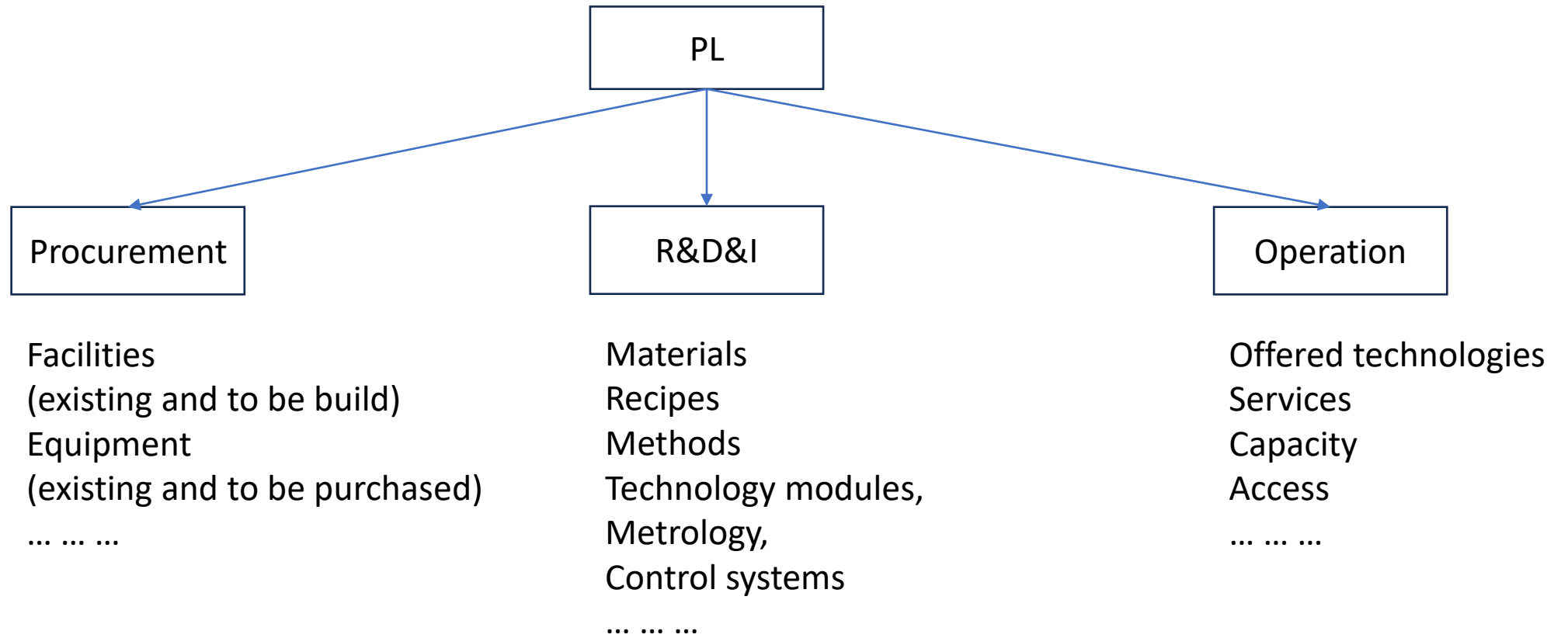
Chips JU PL Calls and Grants

Complete Proposal **PL** Call for Expression of Interest (CfEoI)

Procurement R&D&I Operation

Selection of a Hosting Consortium

Call for Expression of Interest (CfEoI)

Set-up, integration and process development

Call for proposals HE

Operational activities of the pilot line

Call for proposals DEP

HA/JPA

HE Grant

DEP Grant

Chips JU

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Competence Centres

EU support for at least one centre per Member State	Co-investment with Member States and Regions	Supporting industry and public services
Access to design platform and pilot lines	Focus on Semiconductors Skills	A strong European network of Competence Centres

Competence Centres

Main services:

- Have specialised areas of expertise in certain technology, domain, or activities (**specialisation**)

- Facilitate effective use of capacities and facilities, including access to **design platform** and **pilot lines**

- Support interested stakeholders in developing semiconductor solutions (**technology transfer**)

- Address **skills shortage** by offering (access to) **training** on semiconductors, including workforce upskilling and reskilling

- Match user needs with available expertise in network of competence centres and act as **access point to the network**

- **Promote Chips Fund** and facilitate access to venture capital

- **Awareness raising, promoting services, promoting success stories**

Entities Forming Competence Centres and Users

- **Competence centre**: single organisation or coordinated group of organisations with complementary expertise, established with non-profit objective, aiming to promote the use of semiconductor technologies

- Competence centres can be built on established entities in the field or can be set up from scratch

- **Users**: companies, in particular local/national SMEs and startups, RTOs, academic institutions, public authorities

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Funding Model

- European **network of competence centres** in semiconductors, system integration and design shall be established

- Participating States may decide <u>not to nominate</u> any candidate entity to become a competence centre in its territory, or to <u>nominate together with other countries</u> (cross-border competence centre)

- Participating States are expected to **co-finance** their national competence centres **on a 50-50 basis**

- EU funding: **max EUR 1 million per year, per country, for a 4-year period**, provided that same or higher national co-financing is available

Service Offerings

- Access to competence centres' services shall be granted on an open, transparent and non-discriminatory basis

- Services to **SMEs** and **public sector** organisations: **free** or against **reduced prices**

- **Larger companies**: against **market price** or **actual costs**

Selection Process

The selection process would have **two phases**:

1. A **pre-selection / designation** phase by Participating States
2. A **quality assessment (evaluation)** by Chips Joint Undertaking

Duration pre-selection / designation: roughly 6 months

There may be **two calls**:

- First call: **Q2 2024**
- Second call: **Q3 2025** ("filling gaps")

Chips JU Calls Planning

Anton Chichkov

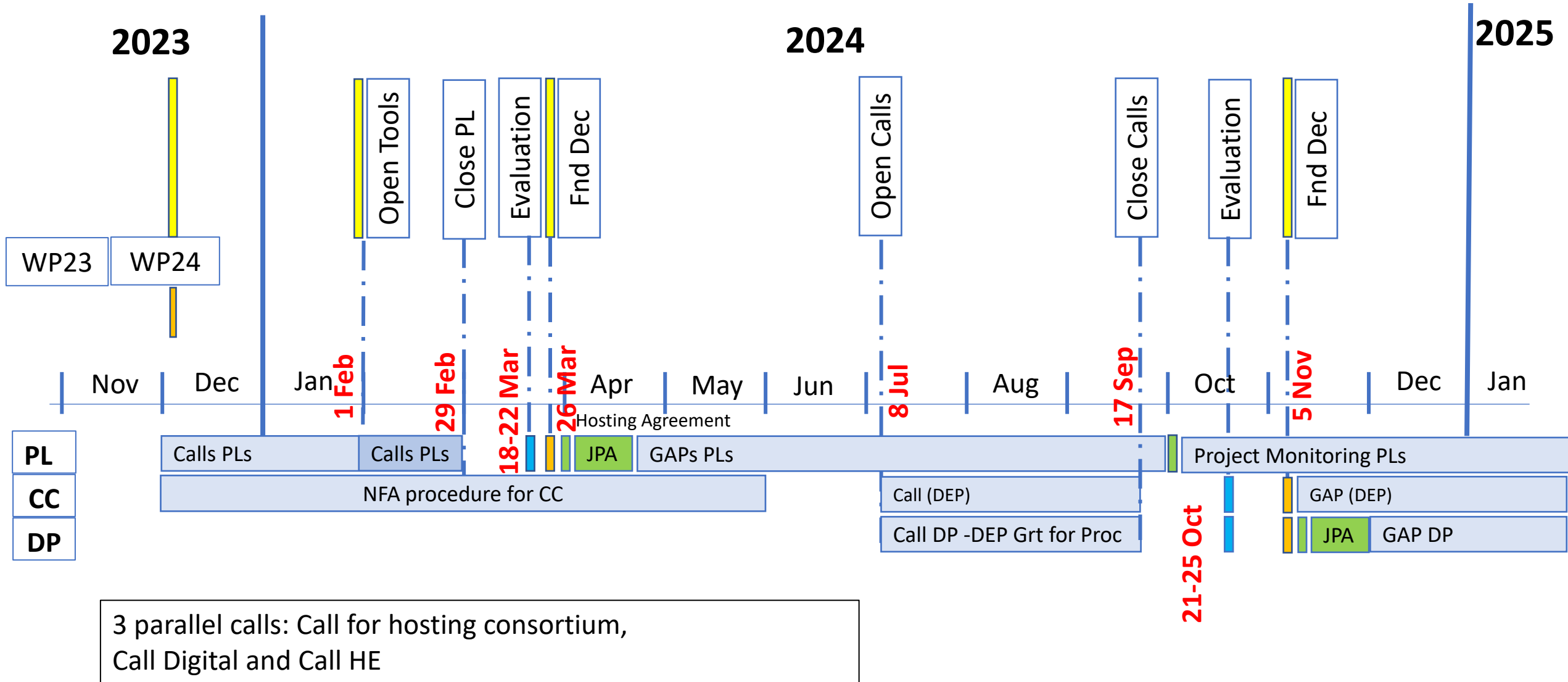Planning Calls 2024 Non-Initiative
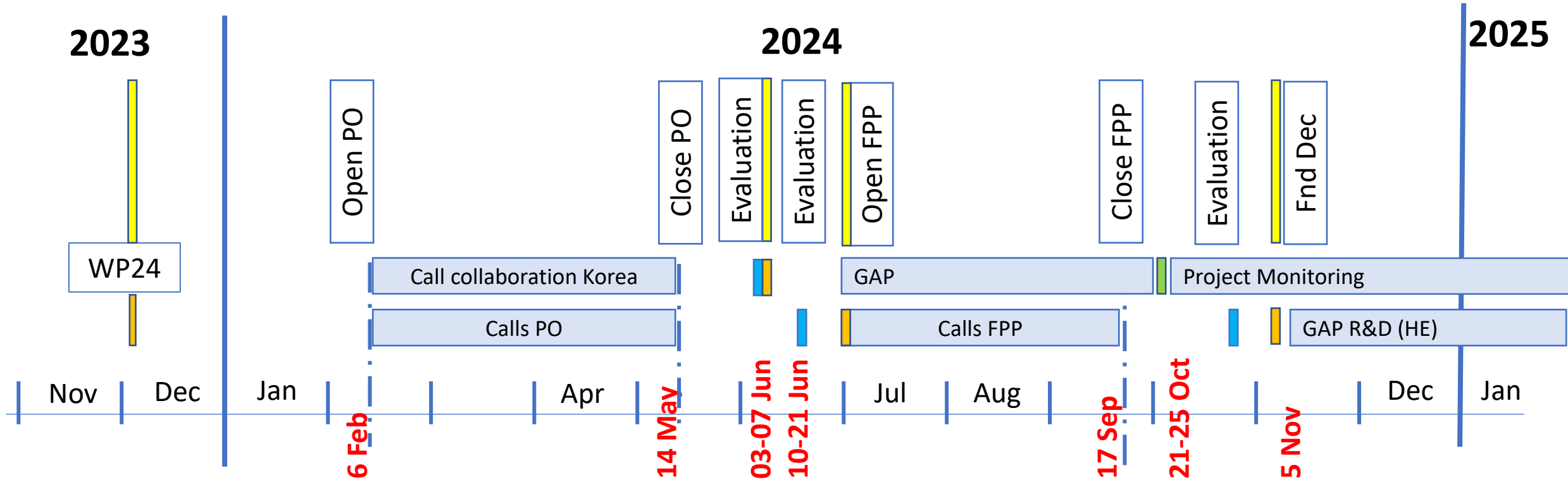
Planning Calls 2023 Initiative
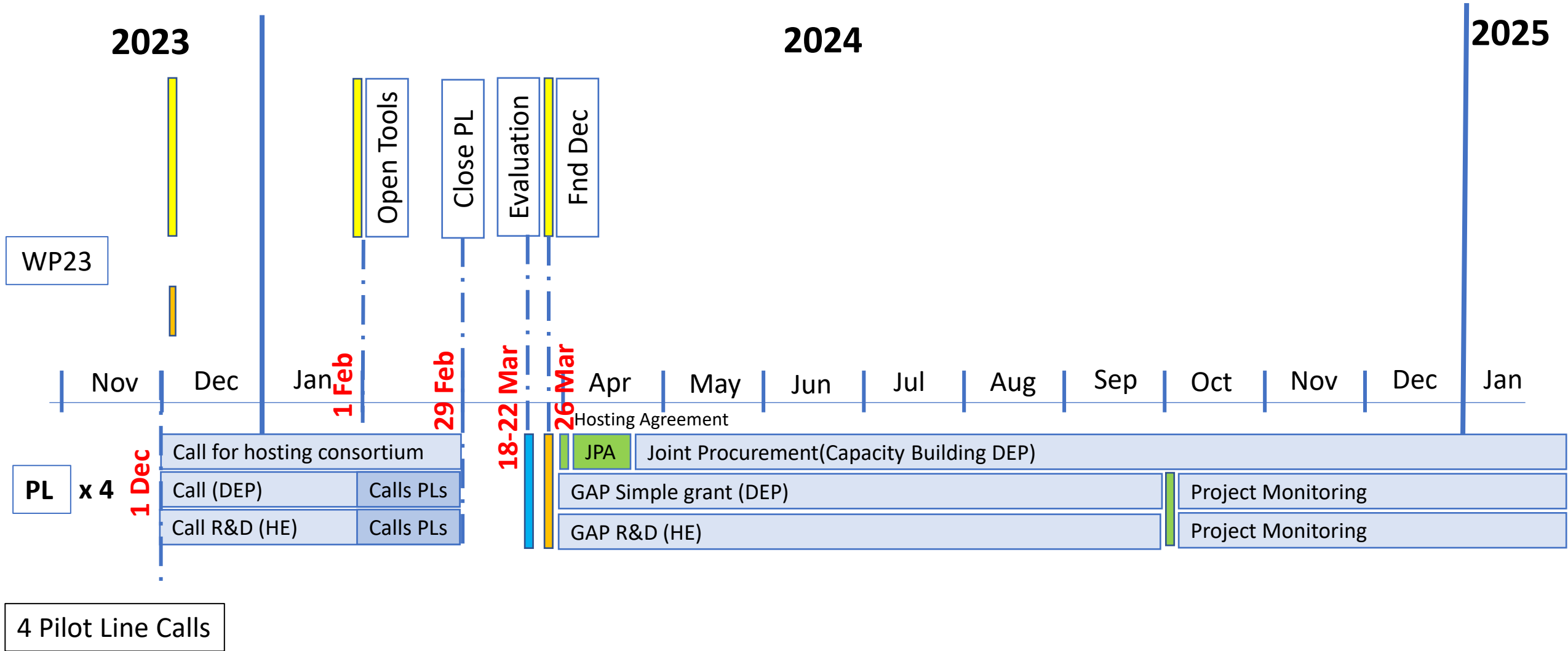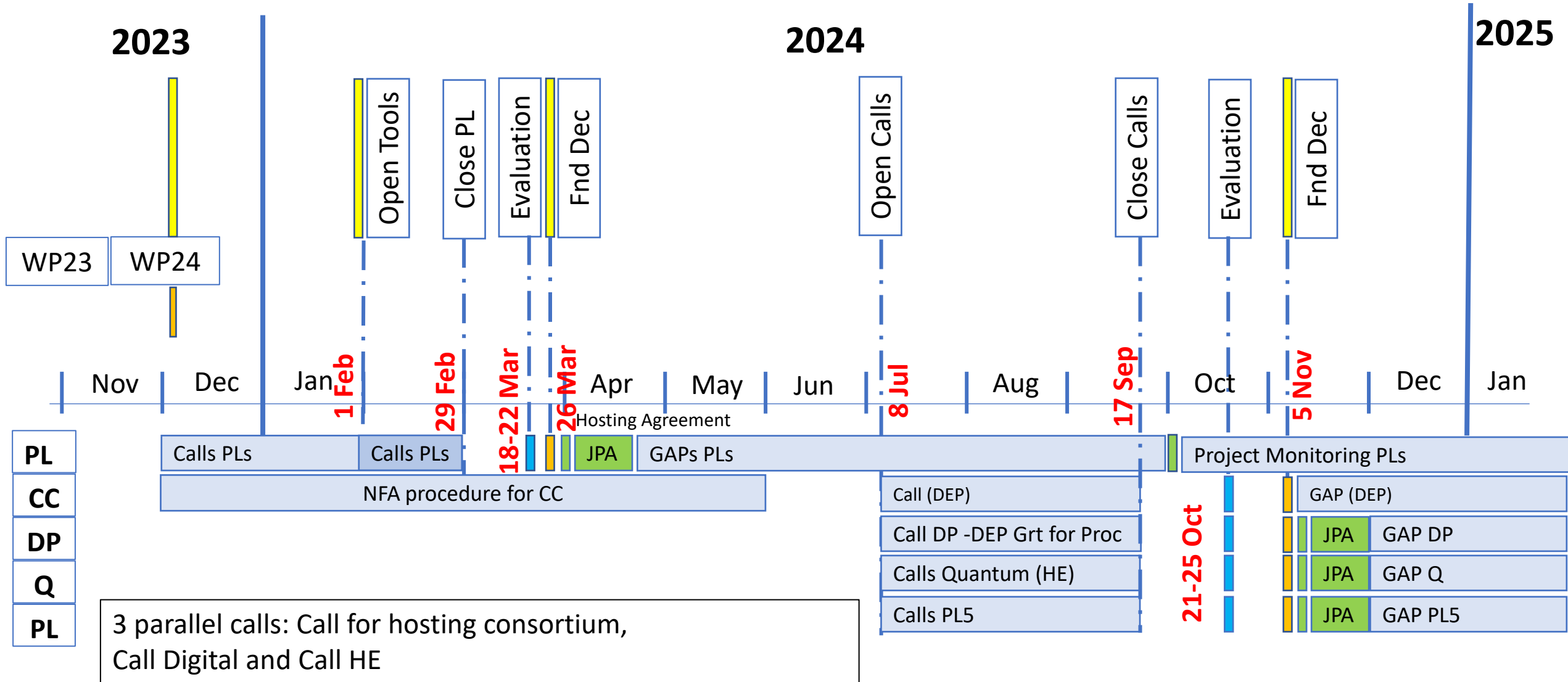
Planning Calls 2024 Initiative
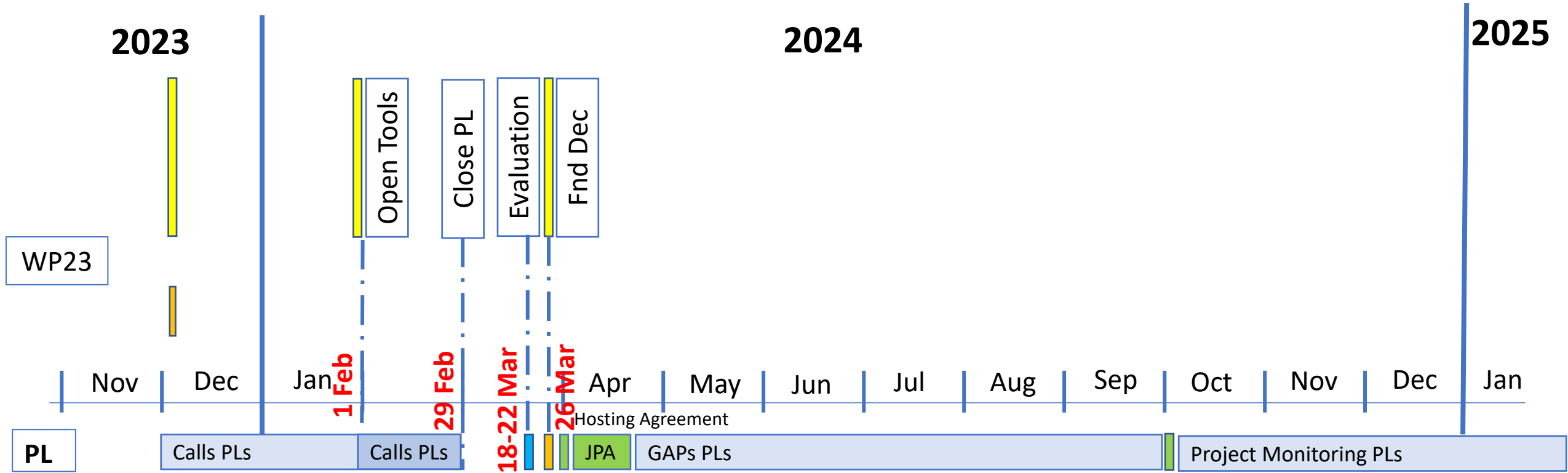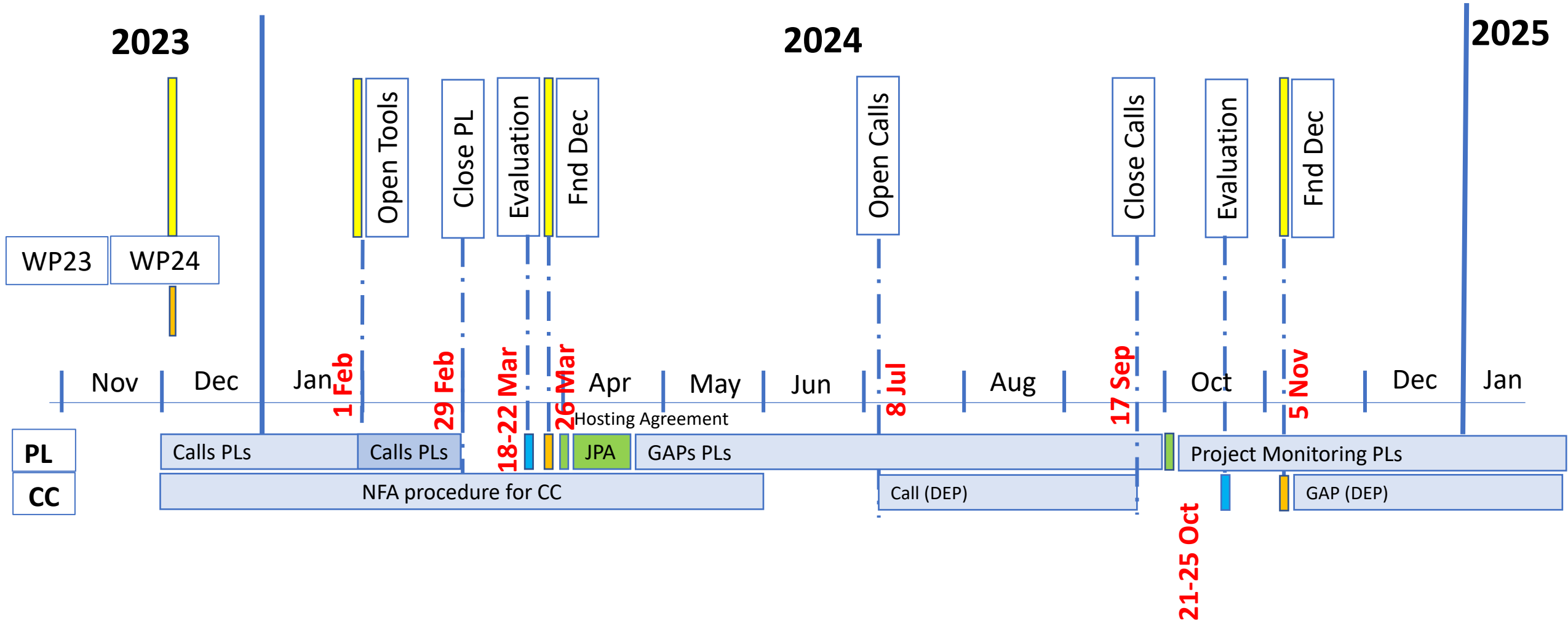
Planning Calls 2024 Initiative

Planning Calls 2024 Initiative

Planning Calls 2024 Initiative

Planning Calls 2023 initiative and 2024 all